October 18, 2002. During the Personal Interview, Applicant's Representative discussed the features of the claimed invention. In view of the discussed issues, Applicant hereby submits the following remarks to further clarify the features of the claimed invention.

The Office Action rejects claims 1-4 and 6-8 under 35 U.S.C. § 112, first paragraph and second paragraph, asserting lack of enablement and indefiniteness, respectively. This rejection is respectfully traversed.

Specifically, the Office Action takes the position that the recitation adjusting the phase of the output signal irrespective of the comparison when starting the delay time adjustment is not described in the specification. Applicant respectfully disagrees.

Independent claims 1 and 3-7 recites adjusting the phase of the output signal irrespective of the comparison when starting the delay time adjustment.

In conventional systems, delays are increased or decreased according to a phase comparison result. That is, delay systems do not only increase the delay. Accordingly, when the dclk signal is in front of the tclk signal, the delay system increases the delay; and when the dclk signal behind the tclk signal, the delay system decreases the delay. However, in a power on condition, the delay is usually set at its minimum. Therefore, a conventional delay system cannot decrease the delay any more than its minimum setting, at power on, resulting in an underflow error.

In contrast, Applicant has devised a system to overcome the above and other deficiencies by using a state detection circuit 22 and a state judgment circuit 20, wherein the delay is increased to bring the dclk signal into the next period of the tclk signal. As stated in the Applicant's claims, the phase comparison is not used at the start of the delay.

As discussed in the Applicant's specification, for example, there are cases where

the phase of the dclk signal is ahead of the phase of the tclk signal (as shown in Fig. 6(b) and (e)), or behind the phase of the tclk signal (as shown in Fig. 7(b) and (e)). In the former situation, the delay system uses the results of a phase comparison between the dclk and tclk to delay (move to the right, as seen in Fig. 6) the dclk signal by a TD amount to match the tclk signal.

However, when the frequency of the input signal is high, the latter situation will arise where delaying the dclk signal by a TD amount will not produce the necessary phase delay, since the dclk signal is already past/behind the tclk signal. In this situation, the inventor has configured a power reset initiated state detection circuit 22 that outputs a signal fstz of a high value (H). The high fstz value triggers the state judgment circuit 20 to output a high upz signal to the delay adjuster 24. This initiates the DLL array 7 to lengthen its delay time by an arbitrary time AD, without reference to any decision by the phase comparator 8. See page 15, lines 29 to page 16, line 8, for example.

Once the lengthening of the delay time has been accomplished in the start of the delay process to where the dclk signal is "in front" of the tclk, the state detection circuit 22 sends a low fstz signal to the state judgment circuit 20 to receive the phase comparator comparison, and to adjust the DLL array 7, accordingly. See Fig. 7(f) and page 13, lines 22-35 and page 15, line 29 to page 16, line 8, for example.

Thus, despite the fact that the phase comparator 8 is connected to the state detection circuit 22 and the state judgment circuit 20, it's comparison result(s) are not used until after the initiation of the delay has commenced (i.e., after starting the delay time adjustment). Therefore, based on the description provided in the specification and the explicit use of the phrase "irrespective of said comparison when starting the delay time

adjustment", Applicant respectfully submits that the subject matter of the rejected claims is supported in the specification, and clearly states the limiting term "starting", to supply to when the comparison is ignored. Accordingly, Applicant respectfully submits that one of ordinary skill would understand how to make or use the invention as described in the specification and as claimed.

In view of the discussion provided above, Applicant respectfully submits that the rejected claims clearly state the intended function and limitations of the invention, as supported in the specification. Additionally, Applicant respectfully submits that, in view of the above explanation, as provided in the specification, one of ordinary skill would be enabled to make or use the invention as claimed. Therefore, the withdrawal of rejection to claims 1-4 and 6-8 is respectfully solicited.

The Office Action rejects claims 1-4 and 6-8 under 35 U.S.C. § 102(e) over Lu (U.S. Patent No. 6,100,735). This rejection is respectfully traversed.

Claim 1 is directed to a delay time adjusting method of adjusting a delay time of an input signal so that a phase of the input signal and a phase of an output signal match each other, based on a comparison between phases of the input signal and the output signal. The method comprises the steps of increasing the delay time to adjust the phase of the output signal irrespective of the comparison when starting the delay time adjustment .

Applicant's independent claim 3 recites a delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the method comprising the step of adjusting the delay time so that, when a phase of a

predetermined rising edge of the output second periodic signal is behind a phase of a predetermined rising edge of the input first periodic signal, the predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, a phase of the rising edge being behind and nearest to the phase of the predetermined rising edge of the output second periodic signal, wherein the adjusting of the delay is irrespective of the comparison when starting the step of adjusting of the delay.

Applicant's independent claim 4 recites a delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the method comprising, a first step of judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of the input first periodic signal, and a second step of increasing the delay time to adjust the phase of the output second periodic signal so that, when the phase of the predetermined rising edge is judged to be behind the phase of the first rising edge in said first step, the phase of the predetermined rising edge and a phase of a second rising edge of the input first periodic signal match each other, the second rising edge being one period behind the first rising edge, wherein the steps of judging and delaying are irrespective of the comparison when starting the delay time adjustment.

Applicant's independent claim 5 recites a delay time adjusting circuit for adjusting a delay time of an input signal so that a phase of the input signal and a phase of an output signal match each other between phases based on a comparison of the input signal and said output signal, the circuit comprising, detecting means for detecting a phase difference

between the phase of the input signal and the phase of the output signal, and delaying means for increasing a delay time of the phase of the output signal irrespective of the detection of phase difference when starting the delay time adjustment until the phase difference becomes N periods, where N is an integer other than zero.

Applicant's independent claim 6 recites a delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the circuit comprising, judging means for judging whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a predetermined rising edge of the input first periodic signal, and delaying means for adjusting the delay time so that, when the phase of the predetermined rising edge of the output second periodic signal is judged to be behind the phase of the predetermined rising edge of the input first periodic signal by the judging means, the predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, a phase of the rising edge being behind and nearest to the phase of the predetermined rising edge of the output second periodic signal, wherein the steps of judging and delaying are irrespective of the comparison when starting the delay time adjustment.

Applicant's independent claim 7 recites a delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the circuit comprising, delaying means for delaying the input first periodic signal so as to

generate the output second periodic signal, phase-detecting means for detecting whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a first rising edge of the input first periodic signal; and adjusting means for controlling the delaying means so that, when the phase of the predetermined rising edge is judged to be behind the phase of the first rising edge by the phase-detecting means, the delaying means delays the phase of the output second periodic signal until the phase of the predetermined rising edge and a phase of a second rising edge of the input first periodic signal match each other, the second rising edge being one period behind the first rising edge, wherein the steps of delaying, phase-detecting and adjusting are irrespective of the comparison when starting the delay adjustment.

Lu discloses a segmented dual delay-locked loop for precise variable phase clock generation. More specifically, Lu discloses a delay time adjusting method that utilizes a coarse DLL and a fine DLL to generate incremental delay adjustments. The DLL, as disclosed by Lu, can only phase compare during the second pulse. The DLL is modified so that phase comparison can only occur when the phase detector is armed by the first pulse. Lu also discloses an arming circuit for the phase detector in the coarse DLL. The arming input prevents phase comparison when low, but allows phase detection when high.

However, Lu does not teach or suggest the adjusting the phase output signal irrespective of the comparison when starting the delay time adjustment. Accordingly, Lu does not teach or suggest ignoring the phase comparison of the first and second periodic signals when starting the delay adjustment. Therefore, Applicant respectfully submits that Lu neither teaches nor suggests all the features recited in claims 1-8. Also, the device as disclosed in Lu cannot perform the functions or remedy the deficiencies addressed by the

Applicant's claimed invention.

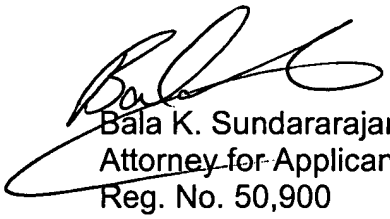
Accordingly, Applicant respectfully submits that Lu does not disclose or suggest all the claimed features of Applicant's invention. Additionally, claims 2 and 8 depend from claims 1 and 7, respectively and are patentable for at least the reasons stated above with respect to claims 1 and 7. Therefore, for at least the above reasons, Applicant respectfully requests the withdrawal of the rejection of claims 1-8 under 35 U.S.C. § 102(e).

In view of the above remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance is earnestly solicited. Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicant respectfully petitions for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to client-matter number 100353-00039.

Respectfully submitted,

Arent Fox Kintner Plotkin & Kahn



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